

Revision : 1.0

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[illegible]

Model Name:GA-78LMT-S2

Component value change history

Version: 1.0

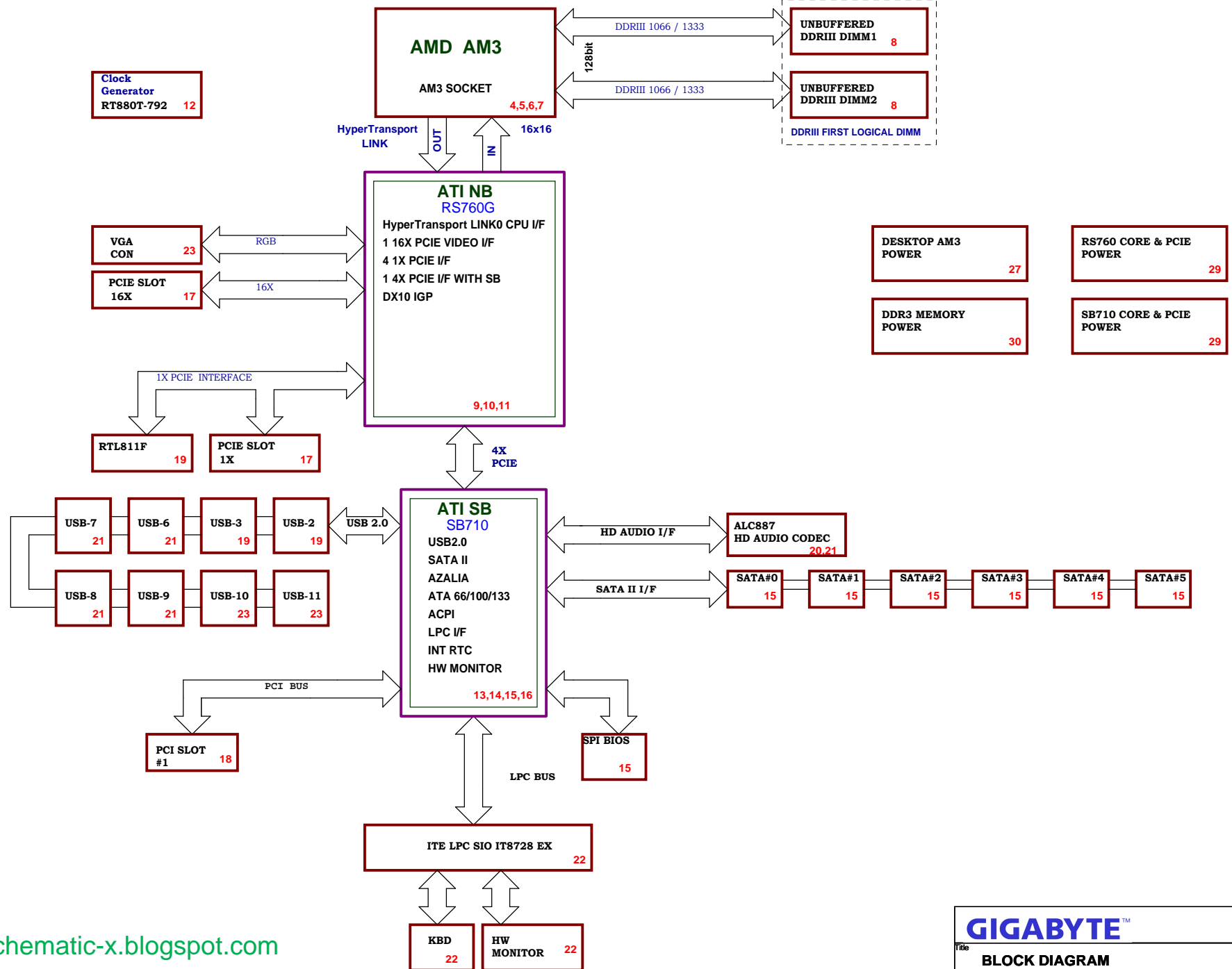
P-Code: U99098-0

[illegible]

Circuit or PCB layout change for next version

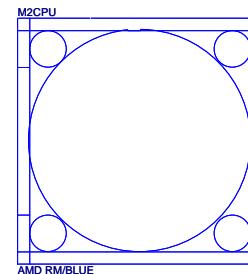
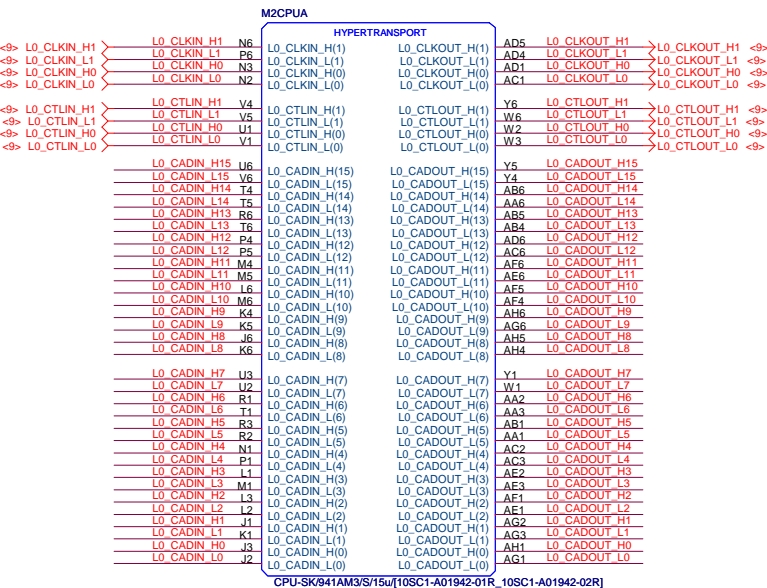
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RS780L CUSTOMER DESKTOP DESIGN



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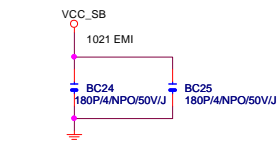
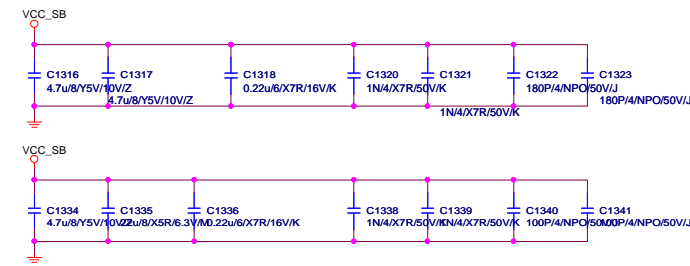
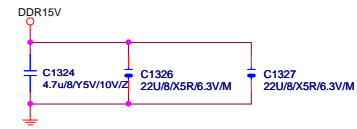
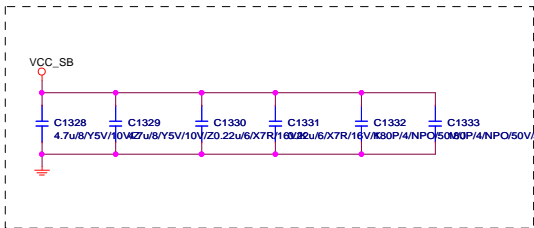
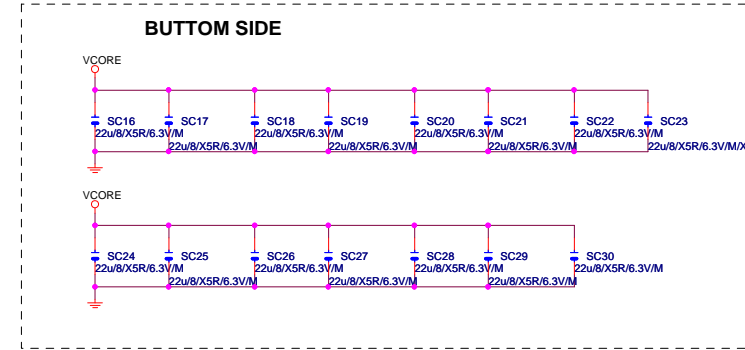
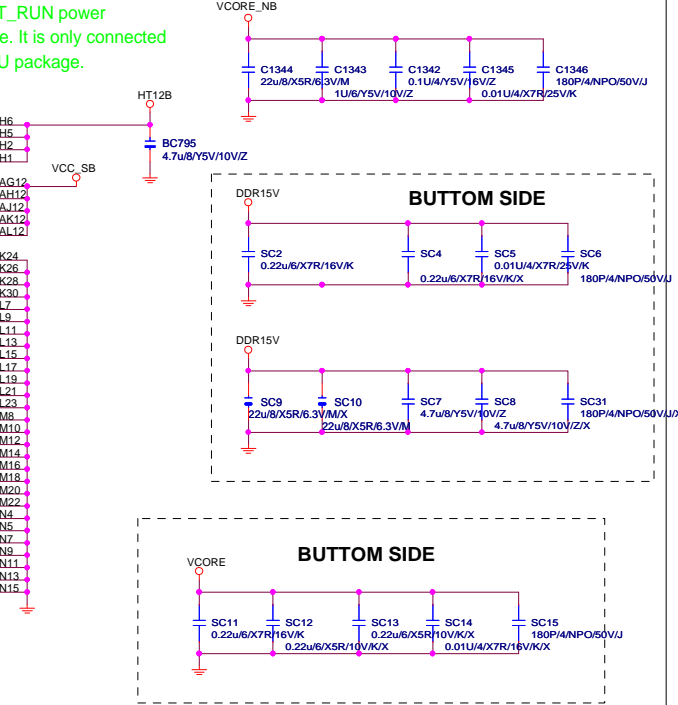
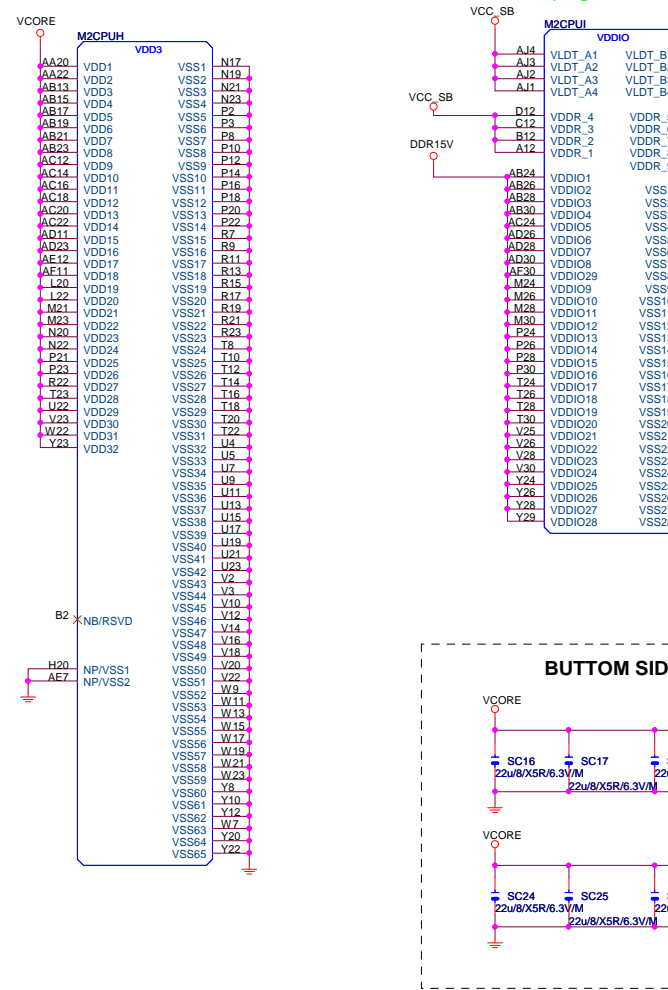
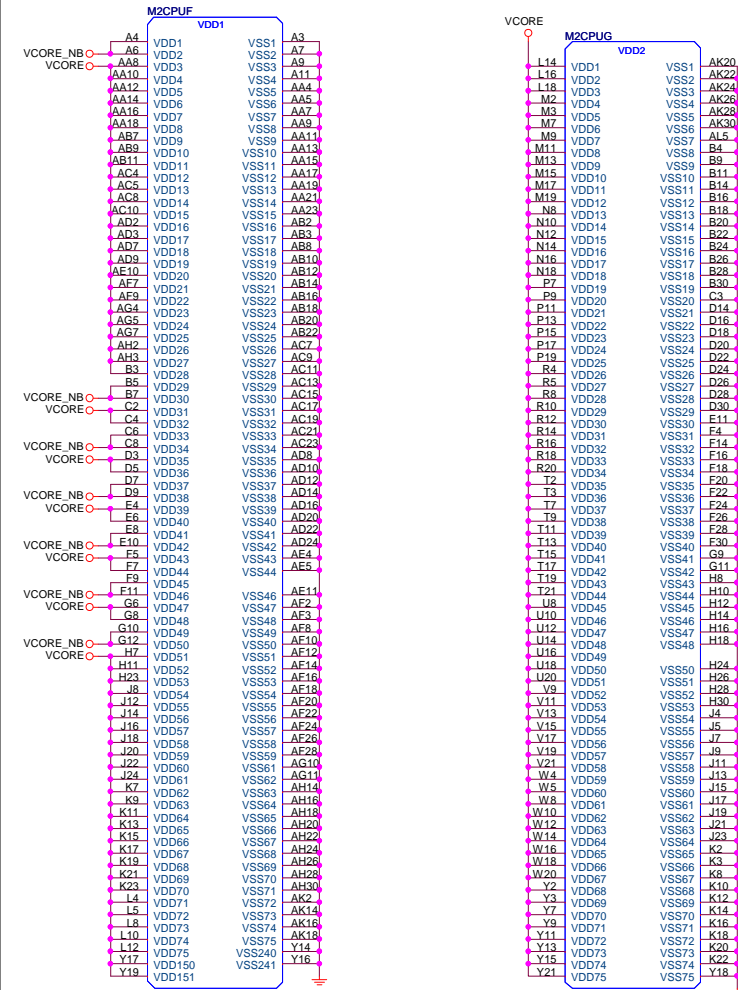
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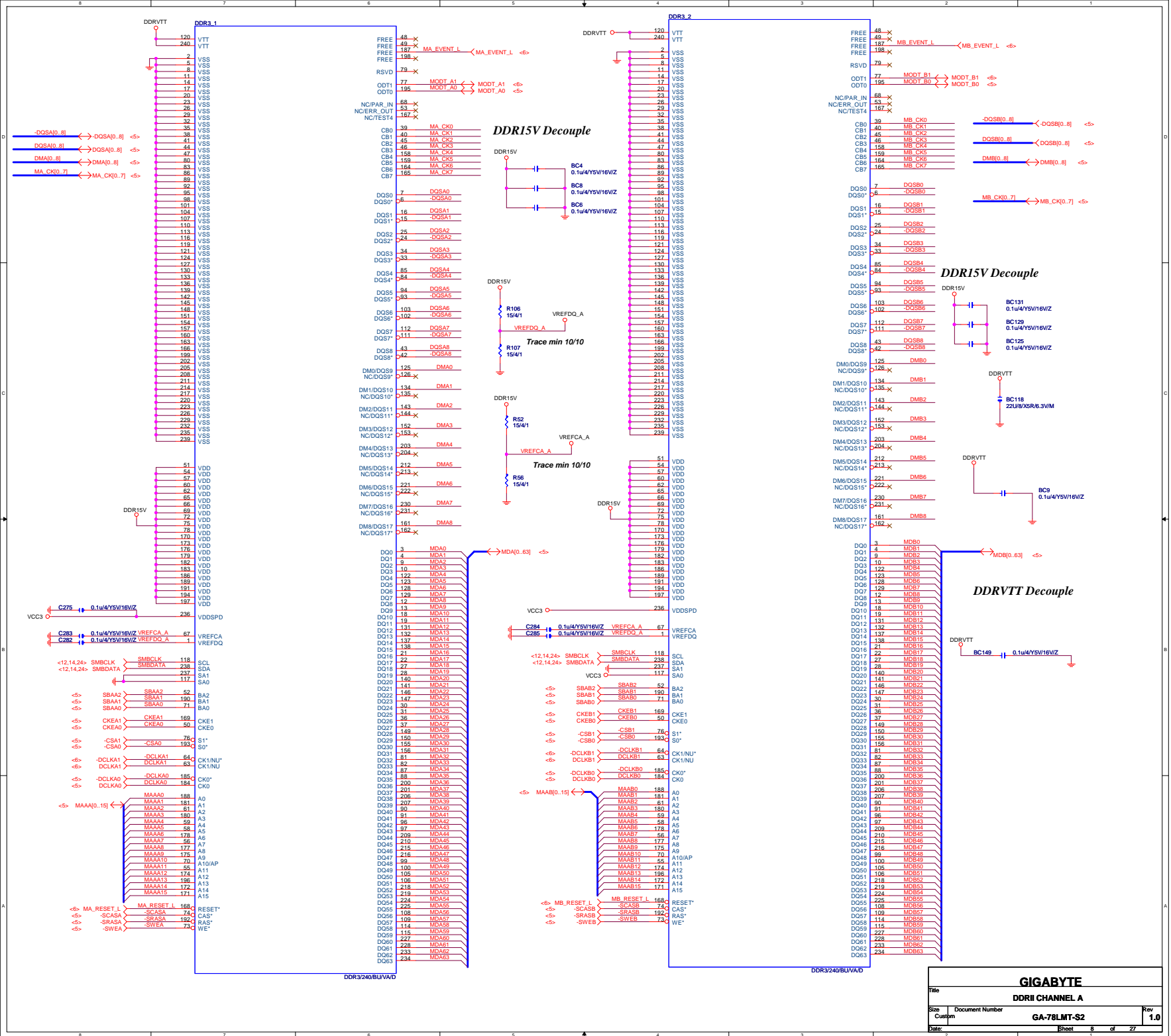


CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

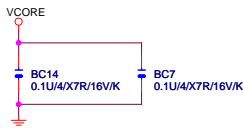




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PART 1 OF 6

HYPER TRANSPORT CPU I/F



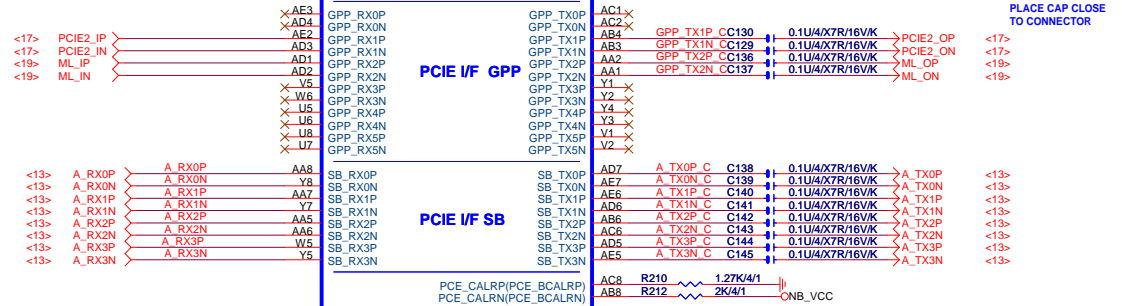
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EXP_A_RXN[0..15] >>>EXP_A_RXN[0..15] <17>
EXP_A_TXP[0..15] >>>EXP_A_TXP[0..15] <17>
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PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB



NB_HS[12SPS-SA0502-01R_12SPS-SA0502-02R]

GIGABYTE™

RS780 HT-LINK I/F

Size: Custom Document Number: GA-78LMT-S2 Rev: 1.0

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RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

RS740_DFT_GPIO1 R272 150/4/1

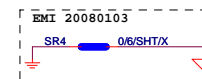
Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

<21> DAC_VSYNCC R276 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly
R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly
R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)



VCC18

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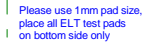
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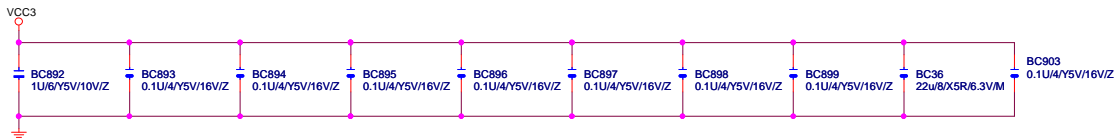
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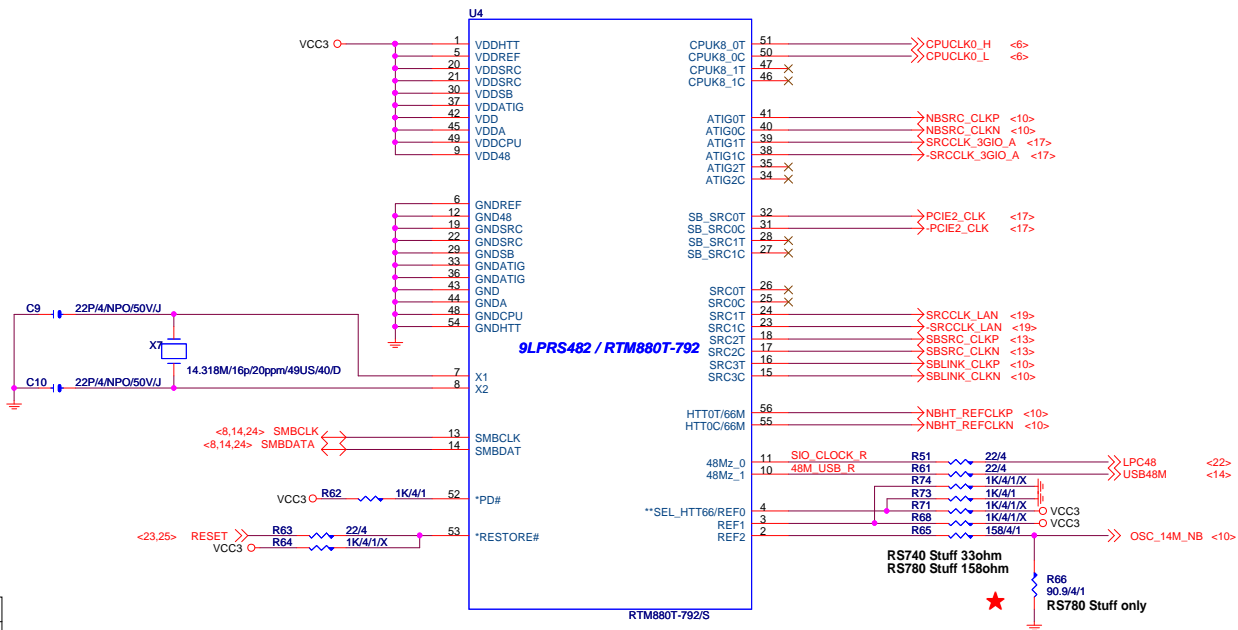


PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDA18PTCIE	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL18T33	+3.3V	NC	NC





- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

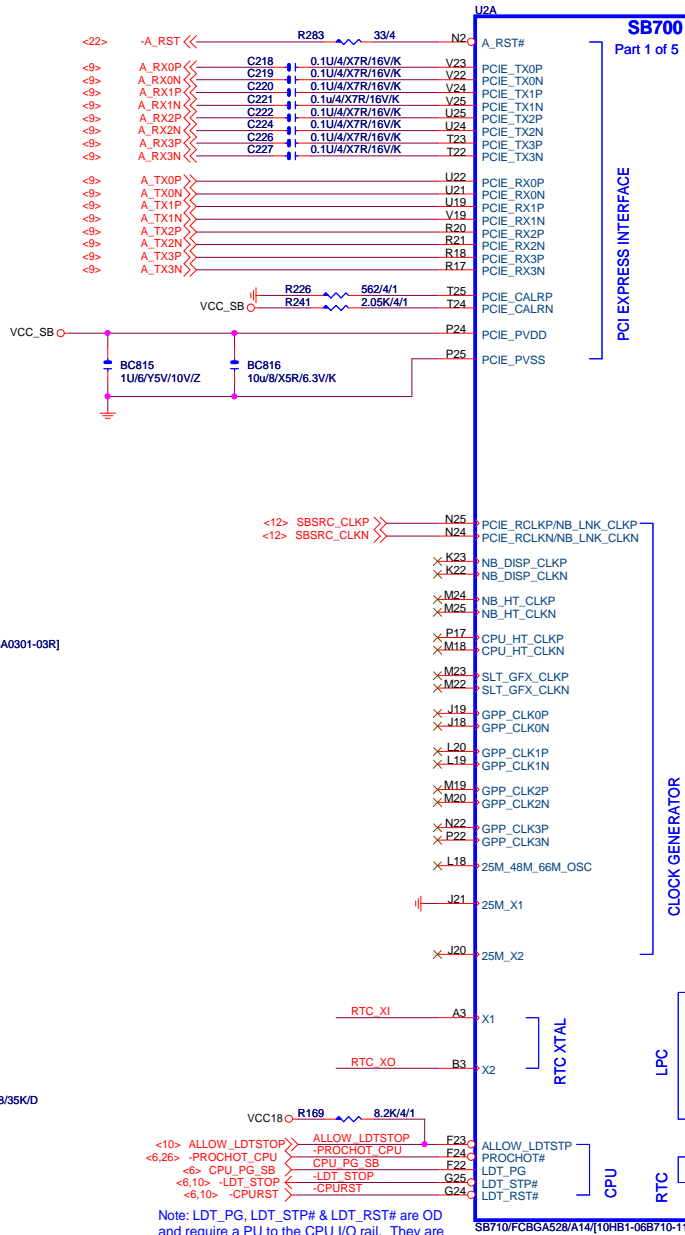
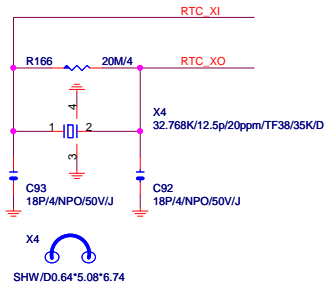
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Title			RTM880T-792	
Size	Document Number	GA-78LMT-S2		Rev
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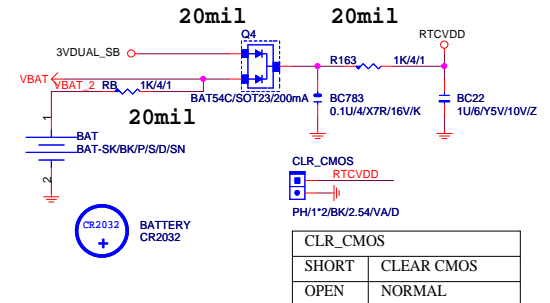
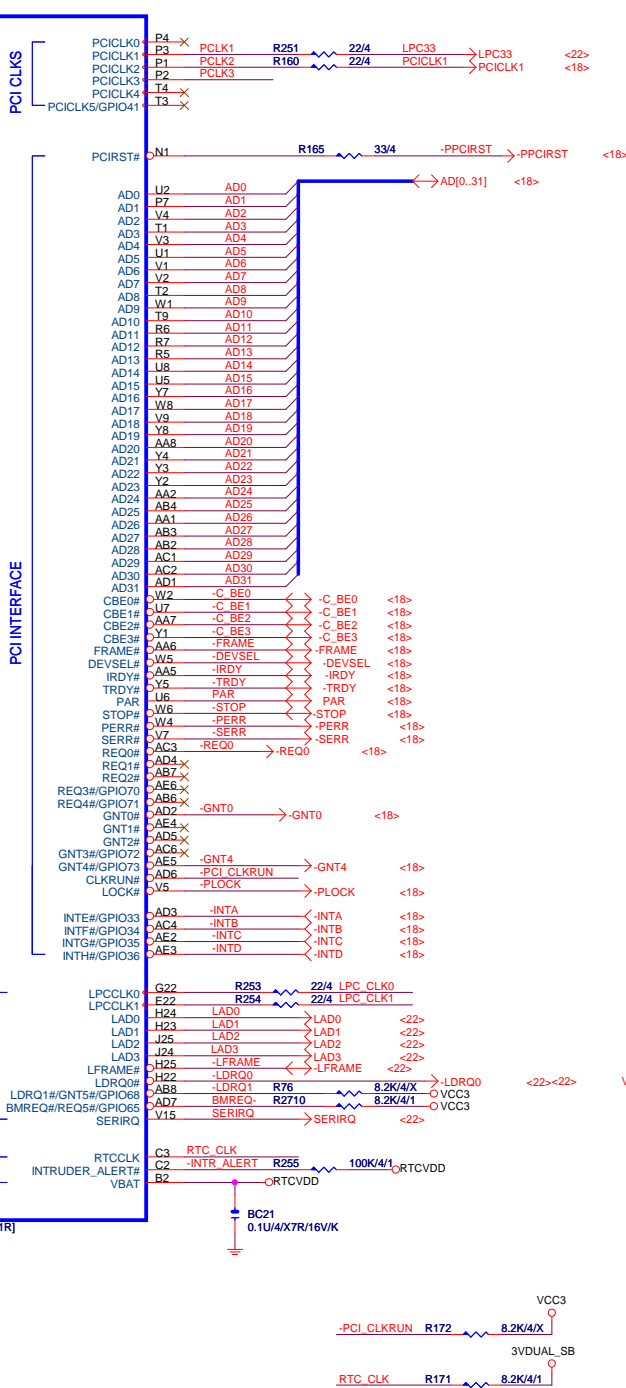
Diagram of a square SB_{HS} with side length 1. The top edge is labeled '1' and the right edge is labeled '2'.

SB_HS/[12SP2-SA0301-01R_12SP2-SA0301-02R_12SP2-SA0301-03R]



Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

SB710/FCBGA528/A14/[10HB1-06B710-11R]

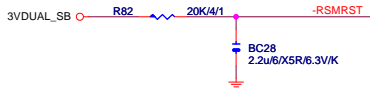
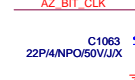
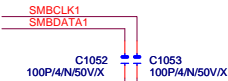
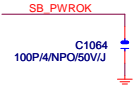
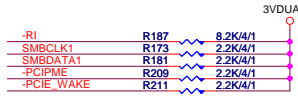
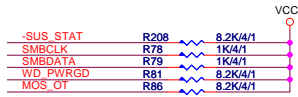


NOT ADD ICT FOR RTCVDD PIN

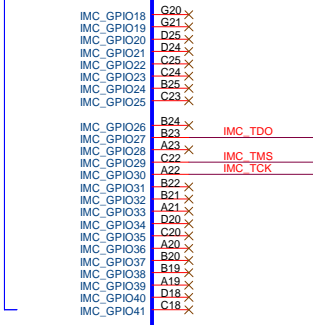
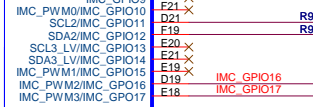
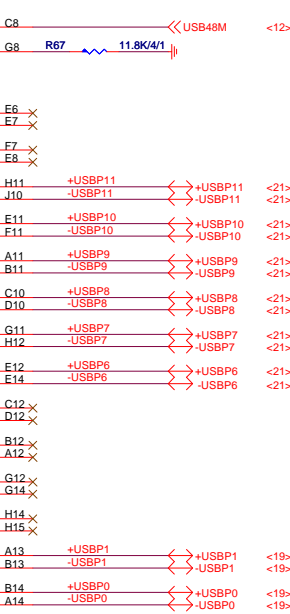
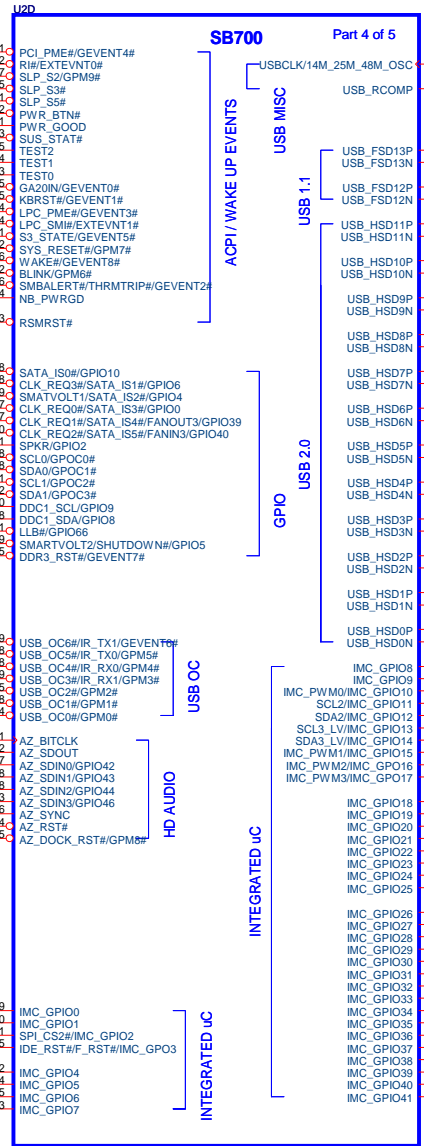
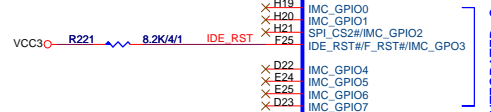
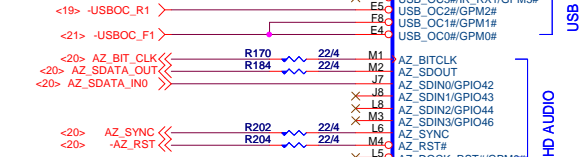
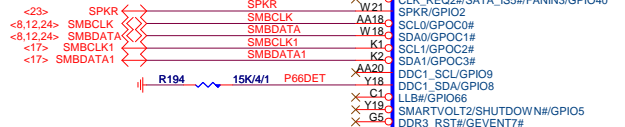
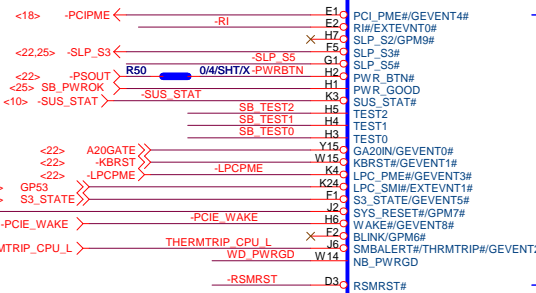
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Title	ATI SB710 PCIE/PCI/CPU/LPC
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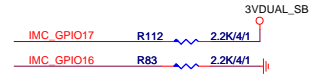


AZ_RST#
 PULL ENABLE PCI
 HIGH MEM BOOT
 PULL DISABLE PCI
 LOW MEM BOOT
 DEFAULT

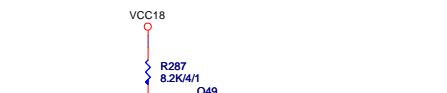
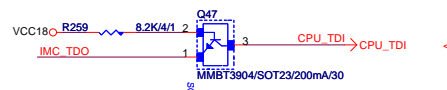


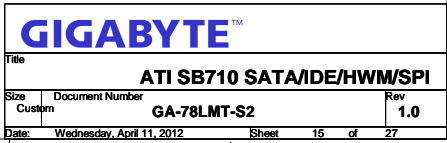
USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

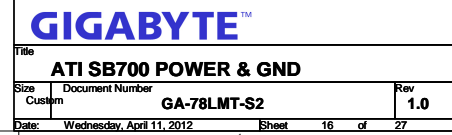
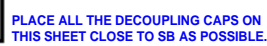
either HWM inputs or PWR_GD signals
 can be used for power-up sequencer

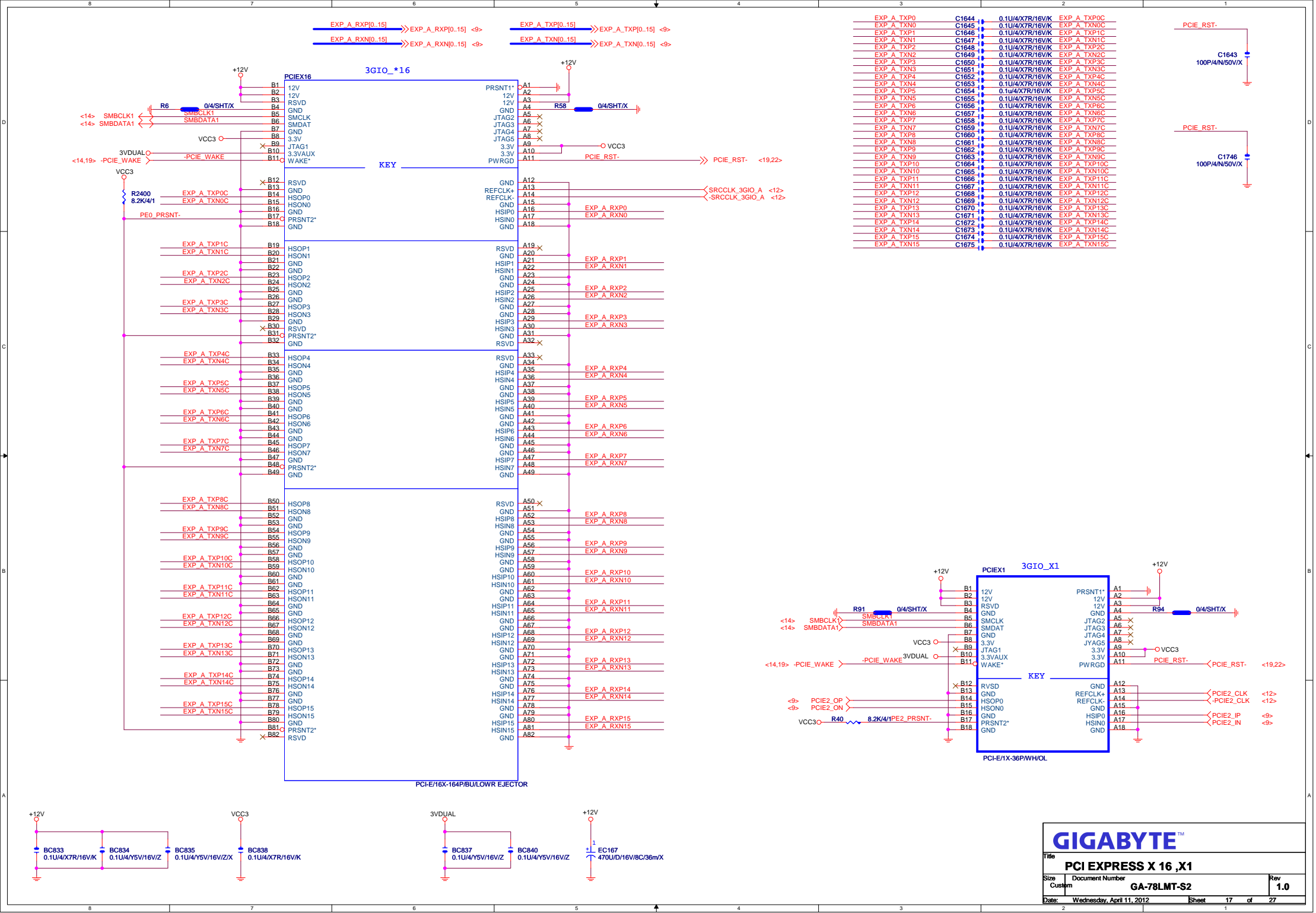


ROM TYPE:
 H, H = Reserved
 H, L = SPI ROM DEFAULT
 L, H = LPC ROM
 L, L = FWB ROM

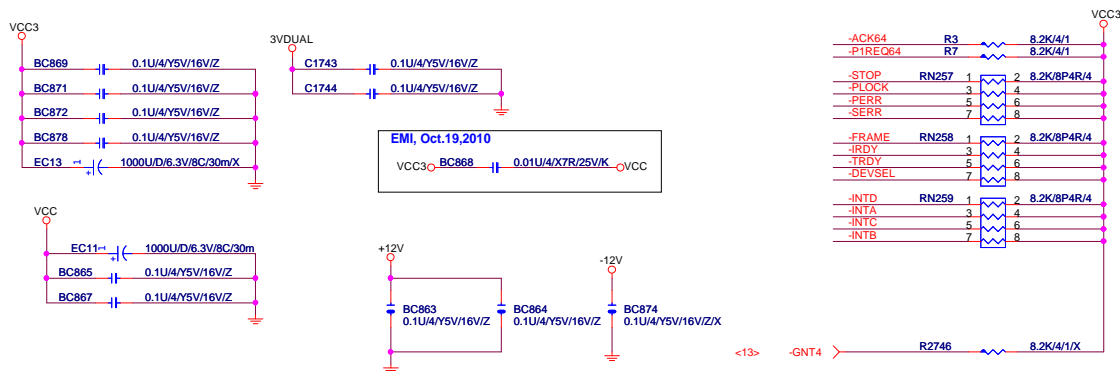
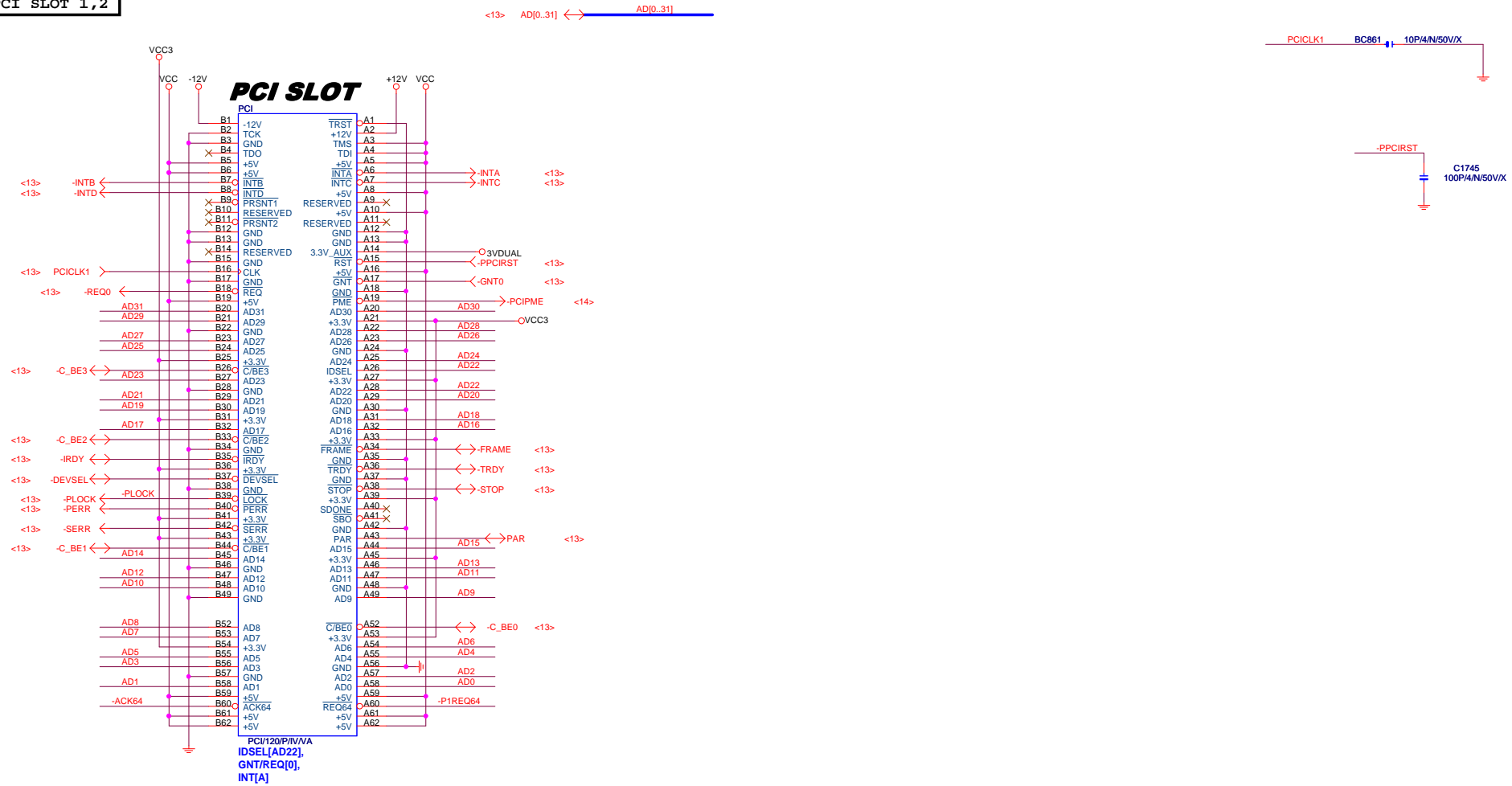






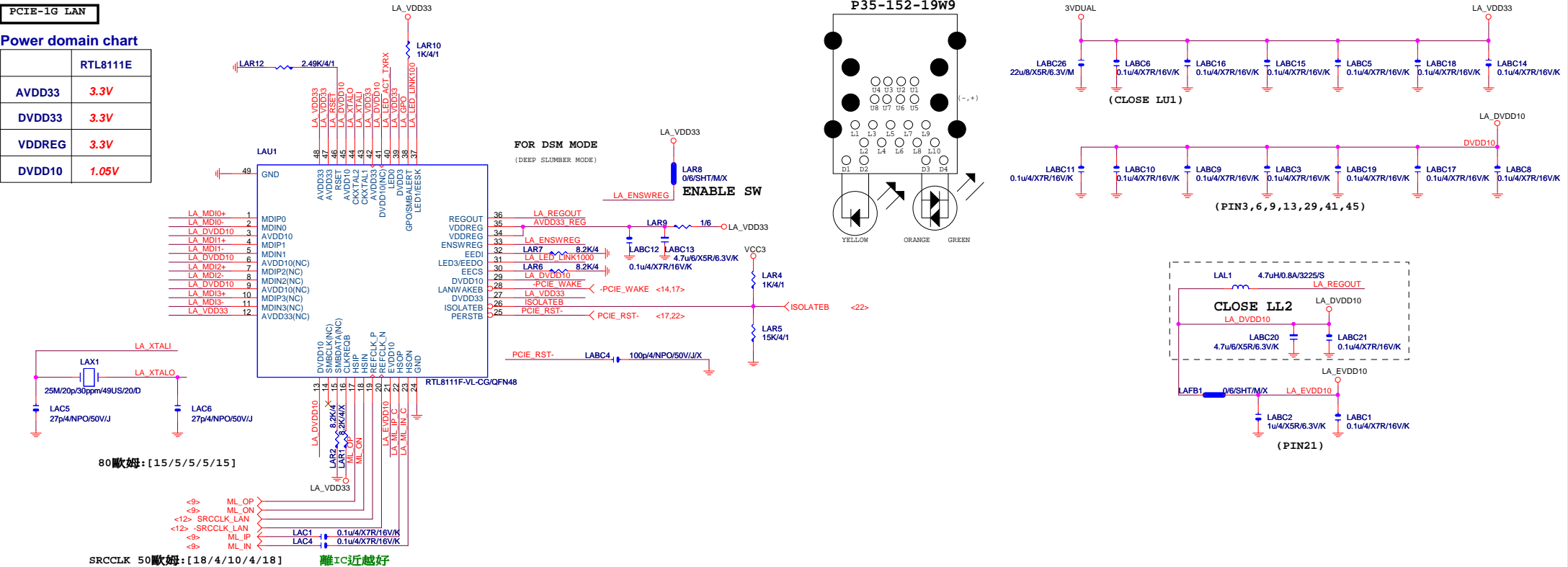


PCI SLOT 1,2

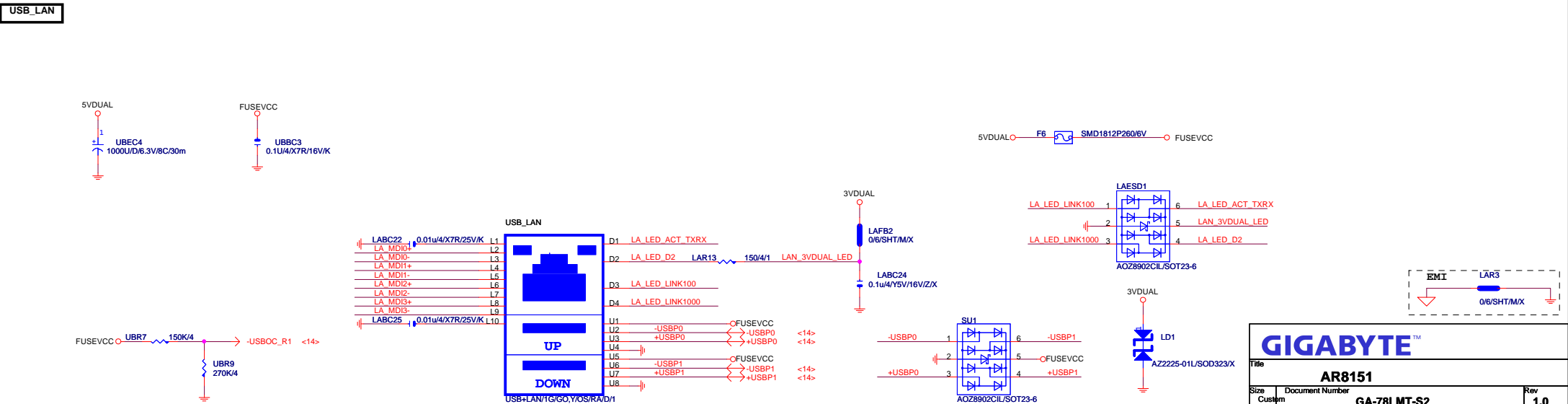


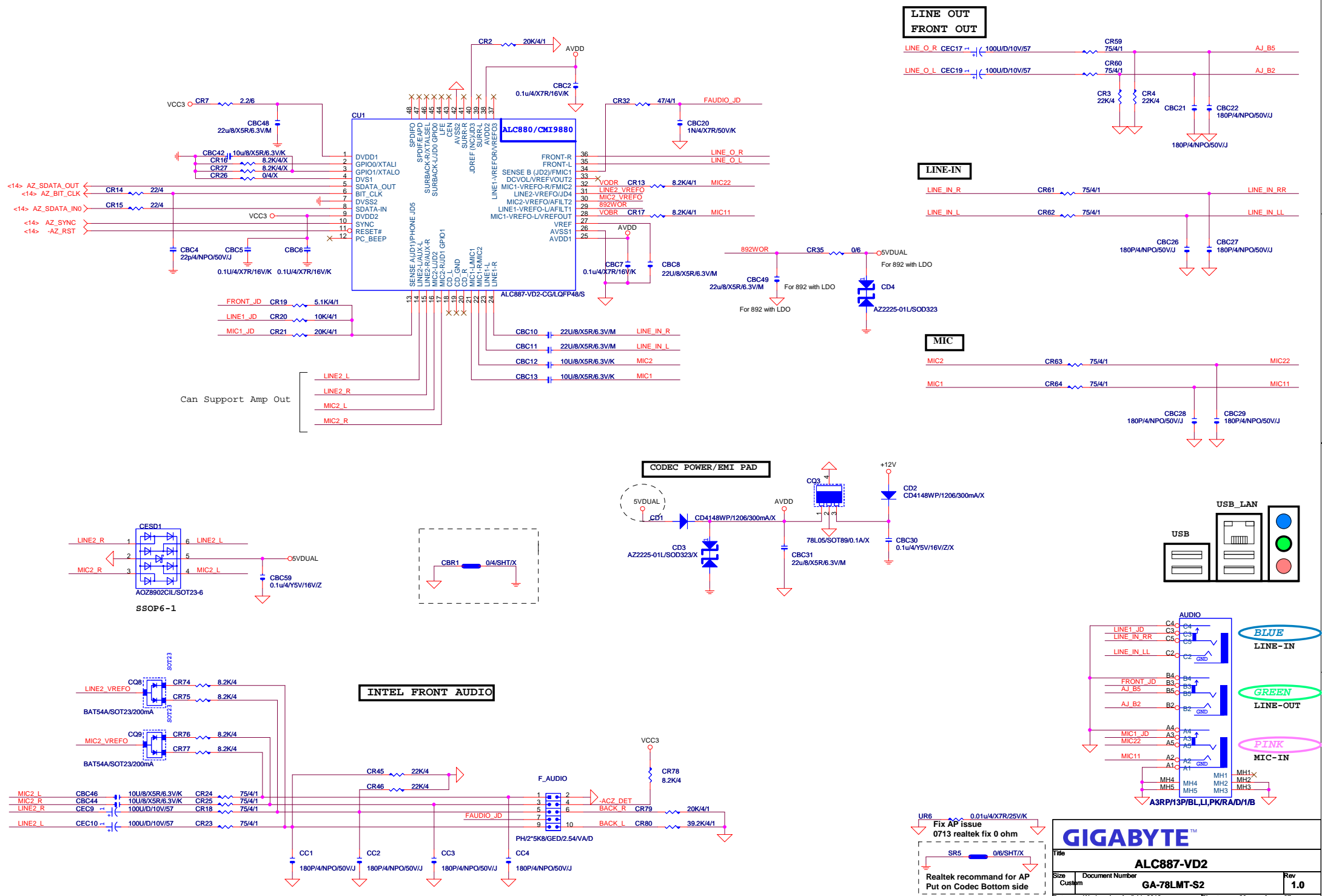
Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

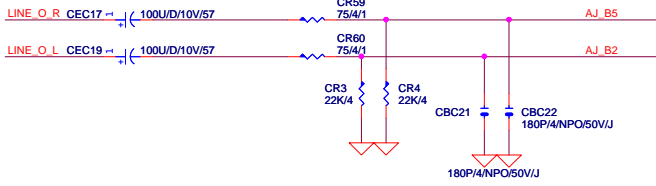


USB_LAN

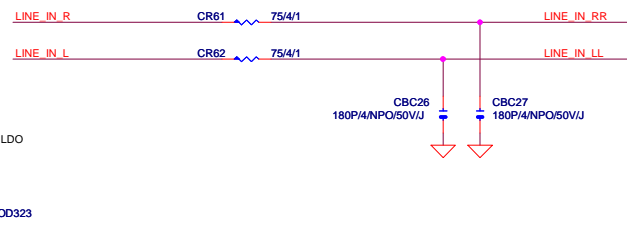




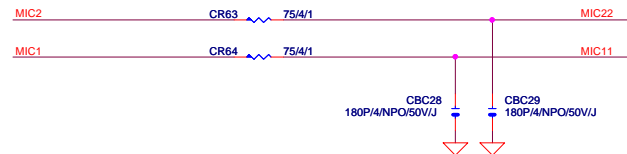
LINE OUT
FRONT OUT



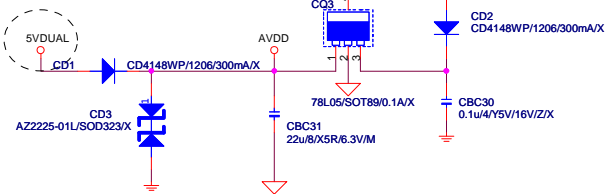
LINE-IN



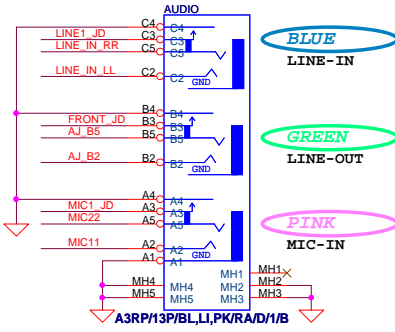
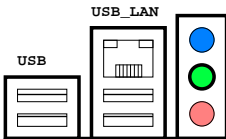
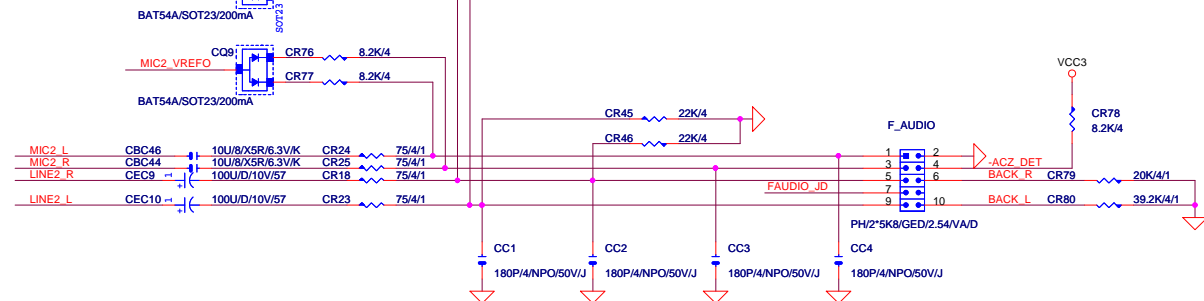
MIC



CODEC POWER/EMI PAD



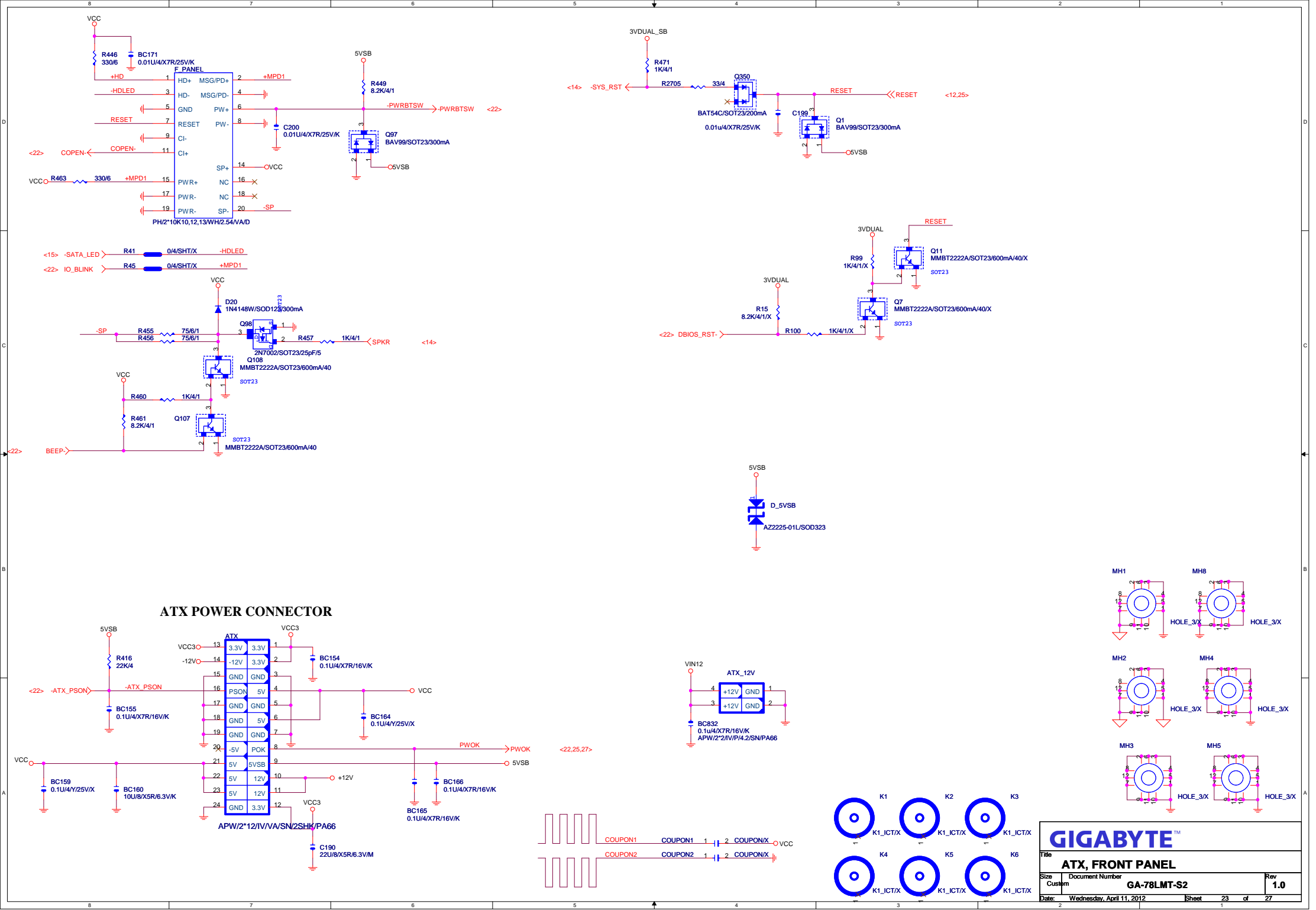
INTEL FRONT AUDIO



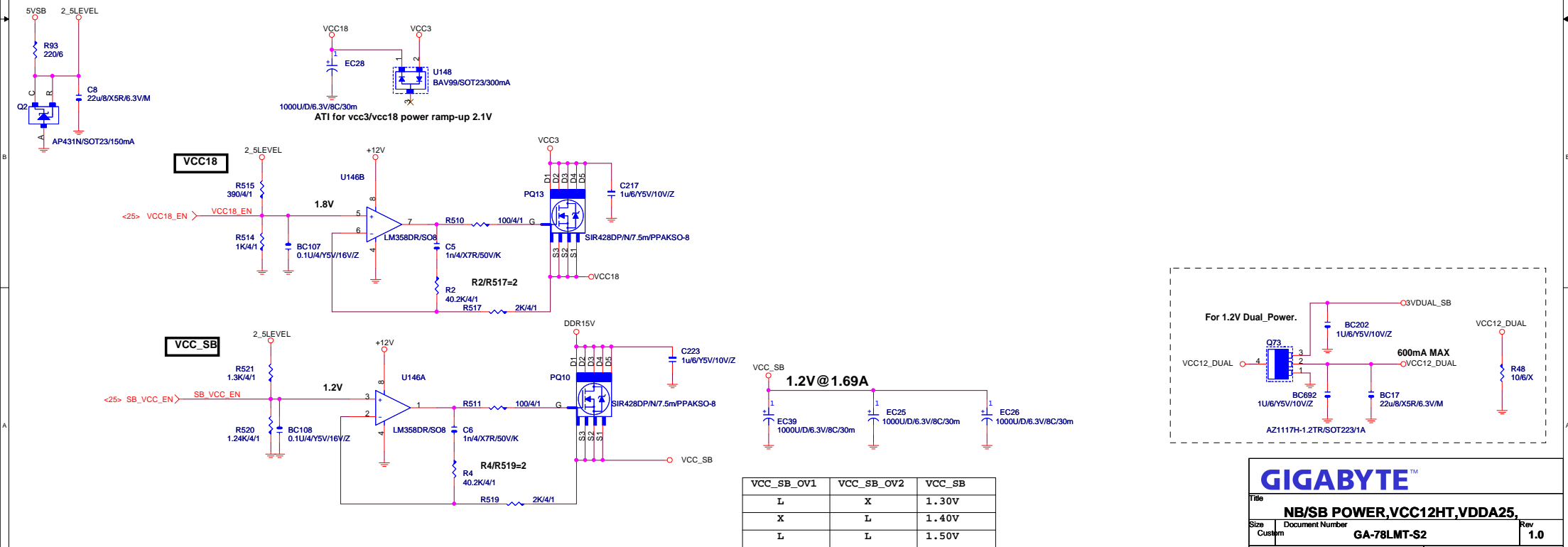
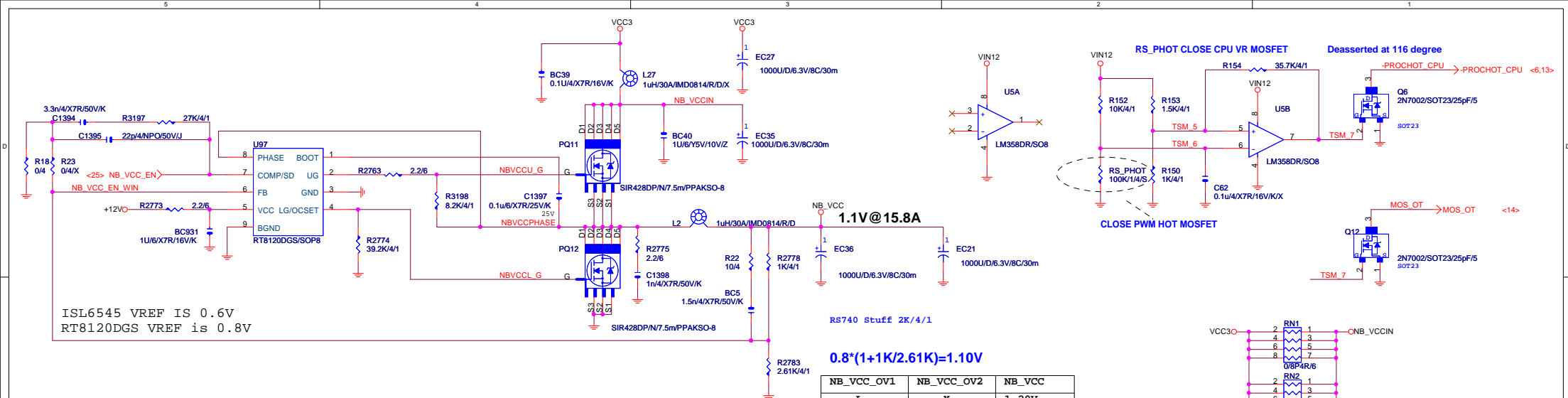
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Date: Wednesday, April 11, 2012	Sheet: 20	of 27

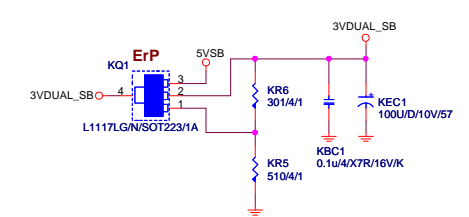
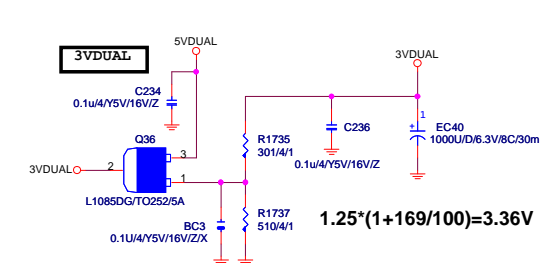
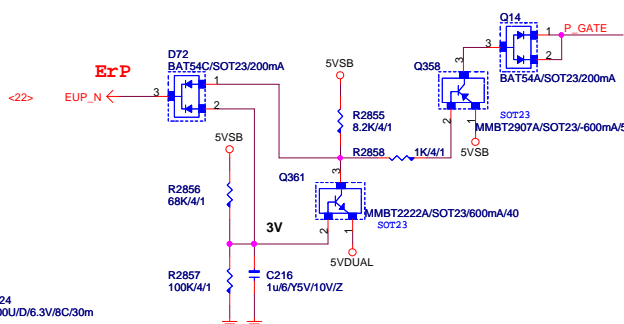
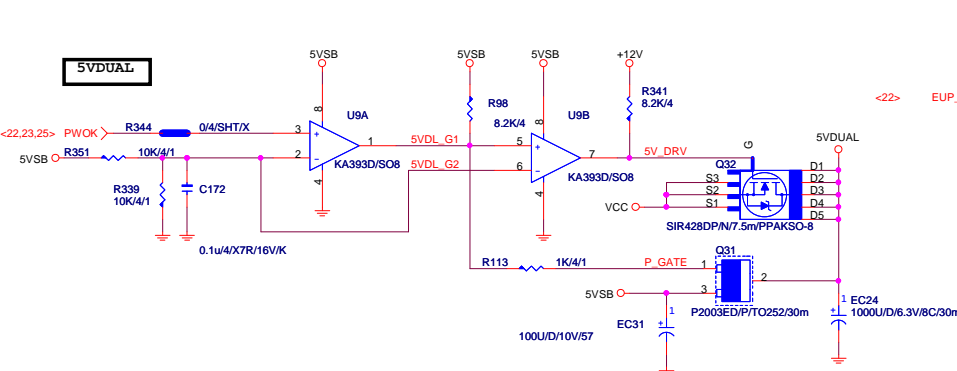












ISL6545 R9=>0, R8=>NC
RT8120 R9=>NC, R8=>0

